MLCC NP0 High Q Series approval sheet

DARFON
Darfon Electronics Corp.

General Specification

General introduction:

Ceramic capacitors (or condenser) are widely used in electronic circuitry for coupling, de-coupling and in filters. These different functions require specific capacitor properties. Ceramic capacitors can be divided into two classes,

- **Class 1**

  In these capacitors dielectric materials are used which have a very high specific resistance, very good Q and linear temperature dependence.

  They are used in such applications as oscillators and filters where low losses, capacitance drift compensation and high stability are required.

- **Class 2**

  These capacitors have higher losses and have non-linear characteristics. They are used for coupling and de-coupling.

Construction:

The capacitance of a ceramic capacitor depends on the area of the electrodes (A), the thickness of the ceramic dielectric (t) and the dielectric constant of the ceramic material (ε_r) ; and on the number of dielectric layers (n) with multi-layer ceramic capacitors :

$$C = \varepsilon_r \times \varepsilon_0 \times A/t \times n$$

The standard capacitance unit is the “Farad”. A capacitor has capacitance of one farad is when one coulomb charges two parallel conductive plate to one volt potential.
The rated voltage is dependent on the dielectric strength, which is mainly governed by the thickness of the dielectric layer and the ceramic structure. For this reason a reduction of the layer thickness is limited. Figure 1 shows the construction of a multi-layer capacitor.
The electrodes are normally mixed palladium with silver since the electrodes are applied before the ceramic is fired at a temperature where silver would oxidize.

Manufacturing of ceramic capacitors

The raw materials are finely milled and carefully mixed. Thereafter the powders are calcined at temperatures between 1100℃ and 1300℃ to achieve the required chemical composition.
Then, the resultant mass is reground and dopes and/or sintering means are added.
The finely ground material is mixed with a solvent and binding matter. Casting or rolling obtains thin sheets. For multi-layer capacitors electrode material is printed on the sheets and after stacking and pressing of the sheets co-fired with the ceramic compact at temperatures between 1000℃ and 1400℃.
The totally enclosed electrodes of a multi-layer capacitor guarantee good life test behavior as well.

Operating Voltage

The operating voltage for the capacitors must always be lower than its rated voltage. If an AC voltage is applied, the peak voltage should be lower than the rated voltage of the capacitor. And if both AC and a pulse voltage may be presented, then the sum of the peak should also be lower than the rated voltage of the capacitor chosen.

E Standard Number

E 3	1.0								2.2								4.7							
E 6	1.0				1.5				2.2				3.3				4.7				6.8			
E12	1.0		1.2		1.5		1.8		2.2		2.7		3.3		3.9		4.7		5.6		6.8		8.2	
E24	1.0	1.1	1.2	1.3	1.5	1.6	1.8	2.0	2.2	2.4	2.7	3.0	3.3	3.6	3.9	4.3	4.7	5.1	5.6	6.2	6.8	7.5	8.2	9.1

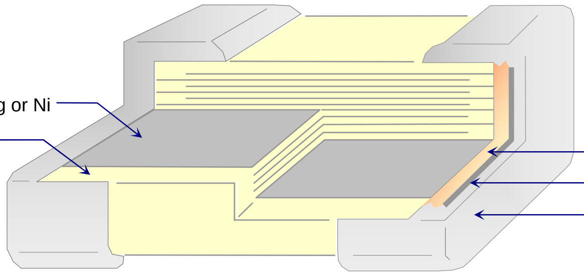
* Non-standard capacitance is available on request.

Available Tolerance

T. C.	Capacitance *	Standard Tolerance	Available Tolerance on Request
NP0 (C0G)	Cap < 5pF	C = ± 0.25pF D = ± 0.5pF	B = ± 0.1pF
	5pF ≦ Cap < 10pF	D = ± 0.5pF	B = ± 0.1pF C = ± 0.25pF
	Cap ≧ 10pF E12	J = ± 5% K = ±10%	F = ± 1% G = ± 2%
X5R X7R	E6	K = ± 10% M = ± 20%	J = ± 5%
Y5V	E3	Z = -20% to +80%	M = ± 20%

* Non-standard capacitance is available on request.

■ **Physical Outline**

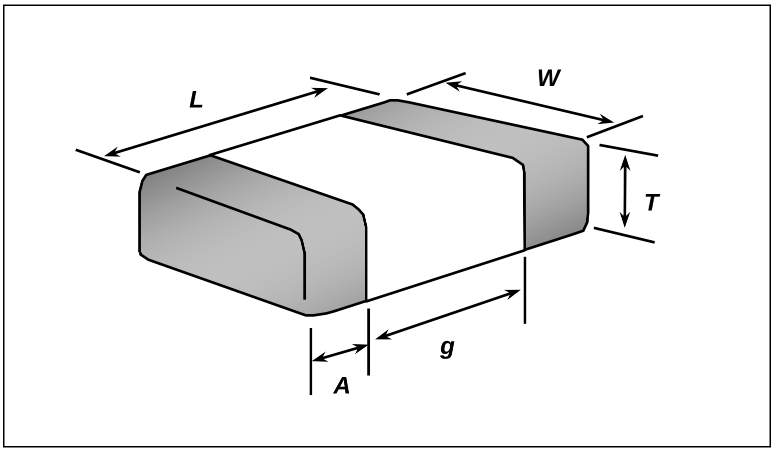


Code	Material Type / Elements	Temperature Compensation Class I		High Permittivity Class II	
		NME*	BME*	NME*	BME*
1	Dielectric	TiO_2	$CaZrO_3$	$BaTiO_3$	$BaTiO_3$
2	Electrode	PdAg	Ni	PdAg	Ni
3	Termination**	Ag	Cu	Ag	Cu
4		Ni			
5		Sn			

* NME (Nobel Metal Electrode), BME (Base Metal Electrode)

** All Darfon's MLCC products are produced under lead-free plating process and in compliance with the lead-free requirement of Green Plan and ROHS.

■ **Dimensions**



TYPICAL TOLERANCE

SIZE CODE (EIA)	L (Length)	W (Width)	T (Max Thickness)	g (Min)	A (Termination Min/Max)	UNIT
0603	0.6+/-0.03	0.3+/-0.03	0.33	0.15	0.10/0.20	mm
(0201)	(0.024+/-0.001)	(0.012+/-0.001)	(0.013)	(0.006)	(0.004/0.008)	(inch)
1005	1.0 +/- 0.05	0.5 +/- 0.05	0.55	0.30	0.10 / 0.30	mm
(0402)	(0.040 +/- 0.002)	(0.020 +/- 0.002)	(0.022)	(0.012)	(0.004 / 0.012)	(inch)
1608	1.6 +/- 0.10	0.8 +/- 0.10	0.90	0.50	0.25 / 0.65	mm
(0603)	(0.063 +/- 0.004)	(0.031 +/- 0.004)	(0.035)	(0.020)	(0.010 / 0.026)	(inch)
2012	2.0 +/- 0.15	1.25 +/- 0.20	1.45	0.70	0.25 / 0.75	mm
(0805)	(0.079 +/- 0.006)	(0.049 +/- 0.008)	(0.057)	(0.028)	(0.010 / 0.030)	(inch)
3216	3.2 +/- 0.15	1.6 +/- 0.20	1.80	1.50	0.25 / 0.75	mm
(1206)	(0.126 +/- 0.006)	(0.063 +/- 0.008)	(0.069)	(0.060)	(0.010 / 0.030)	(inch)
3225	3.2 +/- 0.20	2.5 +/- 0.20	2.70	1.50	0.25 / 0.75	mm
(1210)	(0.126 +/- 0.008)	(0.098 +/- 0.008)	(0.106)	(0.060)	(0.010 / 0.030)	(inch)

SPECIAL TOLERANCE

SIZE CODE (EIA)	L (Length)	W (Width)	T (Max Thickness)	g (Min)	A (Termination Min/Max)	UNIT
1005*	1.0 +/- 0.15	0.5 +/- 0.15	0.65	0.30	0.10 / 0.30	mm
(0402)	(0.040 +/- 0.006)	(0.020 +/- 0.006)	(0.026)	(0.012)	(0.004 / 0.012)	(inch)
1608*	1.6 + 0.15/-0.1	0.8 + 0.15/-0.1	0.95	0.50	0.25 / 0.65	mm
(0603)	(0.063 +0.006/- 0.004)	(0.031 +0.006/-0.004)	(0.037)	(0.020)	(0.010 / 0.026)	(inch)
2012*	2.0 +/- 0.20	1.25 -0.20/+0.30	1.55	0.70	0.25 / 0.75	mm
(0805)	(0.079 +/- 0.008)	(0.049 -0.008/+0.012)	(0.061)	(0.028)	(0.010 / 0.030)	(inch)
3216*	3.2 +/- 0.20	1.6 -0.20/+0.30	1.90	1.50	0.25 / 0.75	mm
(1206)	(0.126 +/- 0.008)	(0.063 -0.008/+0.012)	(0.075)	(0.060)	(0.010 / 0.030)	(inch)
3225*	3.2 +/- 0.30	2.5 +/- 0.30	2.80	1.50	0.25 / 0.75	mm
(1210)	(0.126 +/- 0.012)	(0.098 +/- 0.012)	(0.11)	(0.060)	(0.010 / 0.030)	(inch)

DARFON Part Number

C 1005 NP0 101 J G T S

PRODUCT CODE

C = Capacitor SMD

SIZE in mm (EIA CODE, in inch)

0402(01005)	0603(0201)	1005 (0402)	1608 (0603)	2012 (0805)
3216 (1206)	3225(1210)	4520 (1808)	4532 (1812)	

T. C.

NP0: 0 ± 30ppm/℃	-55℃ to +125℃
X7R: ±15%	-55℃ to +125℃
X5R: ±15%	-55℃ to +85℃
Y5V: +22%/-82%	-30℃ to +85℃

CAPACITANCE CODE

Expressed in pico-farads and identified by a three-digit number.
First two digits represent significant figures.
Last digit specifies the number of zeros.
(Use 9 for 1.0 through 9.9pF： Use 8 for 0.2 through 0.99pF)
(Example: 2.2pF=229 or 0.47pF=478)

TOLERANCE CODE

A: ± 0.05pF	B: ± 0.1pF	C: ± 0.25pF	D: ± 0.5pF	F: ±1%	G: ±2%
J: ±5%	K: ±10%	M: ±20%	Z: +80/-20%		

VOLTAGE CODE

B: 4V	C: 6.3V	D: 10V	E: 16V	F: 25V	N: 35V	G: 50V	H: 100V
J: 200V	K: 250V	L: 500V	M: 630V	P: 1KV	Q: 2KV	R: 3KV	S: 4KV

PACKAGING CODE

T: Paper tape reel Ø180mm (7”)	P: Embossed tape reel Ø180mm (7”)
N: Paper tape reel Ø250mm (10”)	D: Embossed tape reel Ø250mm (10”)
A: Paper tape reel Ø330mm (13”)	E: Embossed tape reel Ø330mm (13”)
B: Bulk, loosed in bag	C: Bulk cassette
W: Special Packing	

Product Type

S: Standard Ceramic Capacitor
Q: High Q/Low ESR

Product Range

- NP0 (Class I)

Type		Size				
T.C.	RV	0603 (0201)	1005 (0402)	1608 (0603)	2012 (0805)	3216 (1206)
NPO Class I	16V			2.7nF~3.3nF		12nF~39nF
	25V	0.20pF~100pF	0.20pF~22pF			
	50V	0.20pF~18pF	0.20pF~470pF/1nF	0.20pF~2.2nF	0.50pF~10nF	1.50pF~10nF
	100V		0.20pF~220pF	0.20pF~1nF	0.50pF~3.3nF	1.50pF~4.7nF

- X7R (Class II)

Type		Size					
T.C.	RV	0603 (0201)	1005 (0402)	1608 (0603)	2012 (0805)	3216 (1206)	3225 (1210)
X7R Class II	6.3V				4.7uF~10uF		
	10V	3.3nF/4.7nF/10nF	100pF~100nF	100pF~1uF	1uF/2.2uF/4.7uF/10uF	2.2uF	
	16V		100pF~100nF	100pF~1uF	330nF/470nF/1uF/ 2.2uF	470nF~10uF	10uF
	25V	100pF~2.2nF	100pF~22nF	100pF~1uF	1nF~1uF	220nF~4.7uF	4.7uF/10uF
	50V	100pF~2.2nF	100pF~10nF	100pF~100nF	150pF~470nF	1nF~1uF	
	100V			100pF~10nF	150pF~22nF	1nF~100nF	

- X5R (Class II)

Type		Size					
T.C.	RV	0603 (0201)	1005 (0402)	1608 (0603)	2012 (0805)	3216 (1206)	3225 (1210)
X5R Class II	6.3V	2.2nF~220nF	470nF~4.7uF	2.2uF/ 4.7uF/10uF	4.7uF~22uF	22uF/47uF	47uF/100uF
	10V	2.2nF~100nF	15nF~1uF	220nF~4.7uF	2.2uF~10uF	2.2uF~10uF	22uF
	16V		15nF~1uF	220nF~2.2uF	1uF~10uF	2.2uF~10uF	4.7uF~22uF
	25V		100nF	220nF/1uF	1uF~4.7uF	2.2uF~10uF	4.7uF/ 10uF

- Y5V (Class II)

Type		Size			
T.C.	RV	0603 (0201)	1005 (0402)	1608 (0603)	2012 (0805)
Y5V Class II	6.3V	22nF~100nF	10nF~1uF	10nF~2.2uF	
	10V		10nF~1uF	10nF~2.2uF	
	16V		10nF~220nF	10nF~2.2uF	100nF~2.2uF
	25V		10nF~100nF	10nF~330nF	100nF ~2.2uF
	50V		10nF~33nF	10nF~220nF	100nF~1uF

Note：(1) Other size, capacitance, and voltage are available upon customer's request.

(2) Product range might be extended due to technology improvement or new product released；for up-to-date information, please contact our sales.

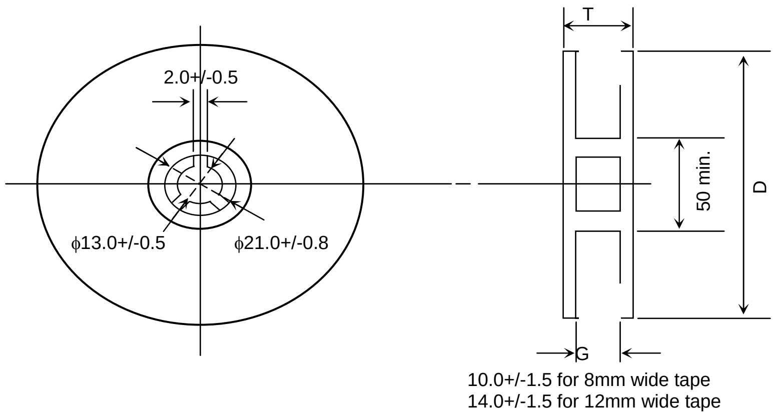
(3) Part of Y5V product will be phased out.

Packaging

- **Tape and Reel Packaging**

Tape and reel packaging is currently the most promising system for high-speed production. A typical 180mm (7 inch) diameter reel contains 1,500 to 15,000 capacitors, 250mm (10 inch) contains 10,000 capacitors, and 330mm(13 inch) contains 10,000 to 50,000 capacitors. Three standard sizes are available in taped and reeled package either with paper carrier tapes or embossed tapes.

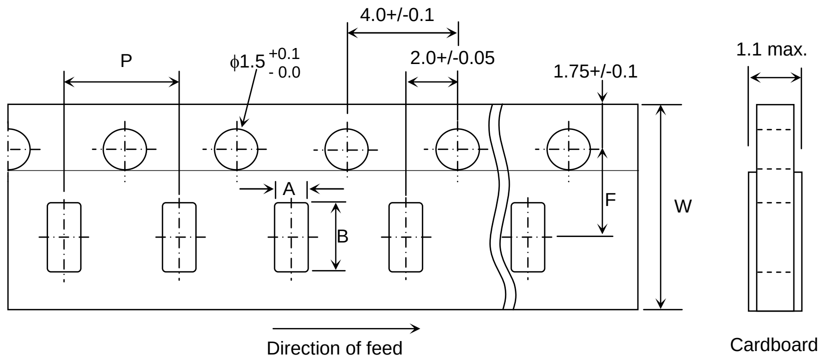
- **Reel Specifications**



TAPE WIDTH (mm)	G (mm)	T max. (mm)	D (mm)
8	10.0 +/- 1.5	14.5	180
8	10.0 +/- 1.5	14.5	250
8	10.0 +/- 1.5	14.5	330
12	14.0 +/- 1.5	18.5	180

- **Paper Tape Specifications**

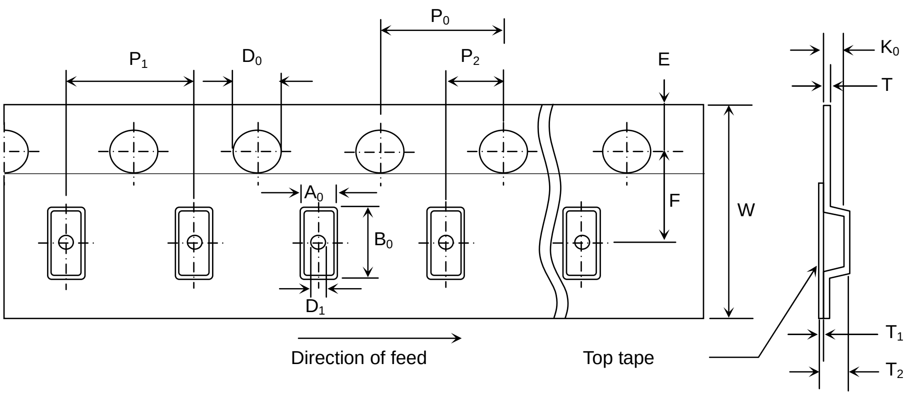
2mm and 4mm pitch tape



SYMBOL	PRODUCT SIZE CODE										UNIT
	0603 (0201)		1005 (0402)		1608 (0603)		2012 (0805)		3216 (1206)		
	SIZE	TOL.	SIZE	TOL.	SIZE	TOL.	SIZE	TOL.	SIZE	TOL.	
A	0.38	+/- 0.04	0.60	+/- 0.04	1.0	+/- 0.2	1.5	+/- 0.2	1.9	+/- 0.2	mm
B	0.68	+/- 0.04	1.12	+/- 0.04	1.8	+/- 0.2	2.3	+/- 0.2	3.6	+/- 0.2	mm
F	3.50	+/- 0.05	3.50	+/- 0.05	3.5	+/- 0.05	3.5	+/- 0.05	3.5	+/- 0.05	mm
P	2.00	+/- 0.10	2.00	+/- 0.10	4.0	+/- 0.1	4.0	+/- 0.1	4.0	+/- 0.1	mm
W	8.00	+/- 0.20	8.00	+/- 0.20	8.0	+/- 0.2	8.0	+/- 0.2	8.0	+/- 0.2	mm

- **Embossed Tape Specifications**

4mm and 8mm pitch tape



k_0: so chosen that the orientation of the component cannot change.
For W= 8mm: T_2=2.5mm max.
For W= 12mm: T_2= 4.5mm

DIMENSION (mm)	PRODUCT SIZE CODE					TOLERANCE (mm)
	4 mm tape			8 mm tape		
	2012 (0805)	3216 (1206)	3225 (1210)	4520 (1808)	4532 (1812)	
P_1	4	4	4	8	8	+/- 0.10
P_O	4	4	4	4	4	+/- 0.10
P_2	2	2	2	2	2	+/- 0.05
A_0 nominal clearance*	0.2	0.3	0.3	0.4	0.4	-
B_0 nominal clearance*	0.2	0.3	0.3	0.4	0.4	-
K_0 minimum clearance*	0.05	0.05	0.05	0.05	0.05	-
W	8.0	8.0	8.0	12.0	12.0	+/- 0.20
E	1.75	1.75	1.75	1.75	1.75	+/- 0.10
F	3.5	3.5	3.5	5.5	5.5	+/- 0.05
D_0	1.5	1.5	1.5	1.5	1.5	+0.1/-0.0
D_1	1 min	1 min	1 min	1.5 min	1.5 min	+0.1/-0.0
T	0.25	0.25	0.25	0.25	0.25	+/- 0.10
T_1	0.05	0.05	0.05	0.05	0.05	+/- 0.01
T_2	2.5 max.	2.5 max.	2.5 max.	4.5	4.5	-

* Typical capacitors displace in pocket.

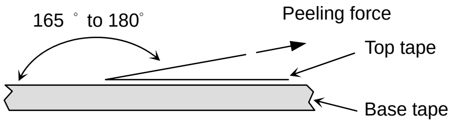
- **Thickness and Taping Amount**

Thickness			Amount per reel					
			180 mm (7”)		250 mm (10”)		330 mm (13”)	
Code	Spec	Size(EIA)	Paper	Embossed	Paper	Embossed	Paper	Embossed
A	0.30+/-0.03	0603 (0201)	15K					
B	0.50+/-0.05	1005 (0402)	10K				50K	
B	0.50+/-0.15	1005 (0402)	10K				50K	
Q	0.45+/-0.05	1005 (0402)	10K				50K	
C	0.60+/-0.15	2012 (0805)	4K		10K		15K	
		3216(1206)	4K		10K		15K	
Q	0.45+/-0.05	1608(0603)	4K		10K		15K	
D	0.80+/-0.10	1608(0603)	4K		10K		15K	
D	0.80+0.15/ -0.10	1608 (0603)	4K		10K		15K	
E	0.85+/-0.15	2012 (0805)	4K		10K		15K	
		3216 (1206)	4K		10K		15K	
		3225 (1210)		3K				10K
		4532 (1812)		1K				
I	0.95+/-0.15	2012(0805)		3K				
		3216(1206)		3K				
F	1.15+/-0.20	3216 (1206)		3K				10K
		4520 (1808)		3K				
G	1.25 +/-0.20	2012 (0805)		2K/3K				10K
		3216 (1206)		3K				10K
		3225 (1210)		3K				
		4520(1808)		3K				
		4532(1812)		1K				
G	1.25+0.3/-0.2	2012(0805)		2K/3K				10K
		3216(1206)		3K				10K
		3225(1210)		3K				
L	1.60+/-0.20	3216(1206)		2K				
		3225(1210)		2K				
		4520(1808)		2K				
		4532(1812)		1K				
L	1.60+0.30/-0.20	3216(1206)		2K				
		3225(1210)		2K				
		4520(1808)		2K				
		45321812)		1K				
N	2.00+/-0.20	3216 (1206)		2K/3K				
		3225 (1210)		2K				
		4520 (1808)		1K				
		4532(1812)		1K				
N	2.00+/-0.30	3225 (1210)		2K				
P	2.50+/-0.20	3225(1210)		500pcs/1K				
P	2.50+/-0.30	3225(1210)		500pcs/1K				

- **Peeling Off Force**

Peeling off force: 0.1N to 1.0N in the direction shown below.

The peeling speed: 300+/-10 mm/min



1. The taped tape on reel is wound clockwise. The sprocket holes are to the right as the tape is pulled toward the user.
2. There are minimum 150 mm as the leader and minimum 40 mm empty tape as the tail be attached to the end of the tape.

High Frequency NP0 (C0G) Dielectrics

Features

- High Q, low ESR
- A monolithic structure ensures high reliability and mechanical strength.
- 0603 (EIA 0201) Ultra-miniature size
- Suitable for high speed SMT placement on PCBs.
- Lead-Free Terminations
- Ni barrier termination highly resistance to migration.
- Lead-free termination is in compliance with the requirement of green plan and ROHS.

Applications

- Cellular Phone, Cordless Phone
- GPS, VCO, RF Integrated Circuits
- Wireless LAN, RF Transceivers
- Communication Equipment
- Custom Applications

High Frequency C0G (NP0) Dielectric Characteristics

Capacitance Range	0.2pF ~ 22pF
Size	0603 (0201) 1005 (0402) 1608 (0603)
Test Voltage	1.0 ± 0.2Vrms
Test Frequency	1.0 ± 0.2MHz
Capacitance Tolerance	± 0.25pF for cap＜5pF (± 0.1pF available on request) ± 0.50pF for 5pF≦cap＜10pF (± 0.1pF, ± 0.25pF available on request) ± 5% for cap≧10pF (± 1%, ± 2% available on request)
Operating Temperature Range	-55℃ to +125℃
Temperature Coefficient	0 ± 30 ppm/℃ (EIA C0G)
Rated Voltage	16, 25 & 50 VDC
*Quality Factor @1MHz	30pF min.: Q≧1000 30pF max.: Q≧400+20C C: Nominal Capacitance (pF)
Insulation Resistance (+25℃, RVDC)	10 GΩ min.
Q & ESR @1GHz	See RF Characteristics of NP0 Q series P:5~7

* Measurements are performed on HP4287A with fixture 16196A (for 1608) / 16196B (for 1005) / 16196C (for 0603), 0.5V; Environment 25℃+/-3℃, 30%~75%RH

■ NP0 – Low ESR/ High Q (Q Series)

CLASS	Class I					
TYPE	Low ESR/High Q					
T.C.	NP0(C0G)					
SIZE	0603		1005		1608	
(EIA)	0201		0402		0603	
RV	25V	50V	25V	50V	25V	50V
* 0.20 p	A	A	B	B	D	D
* 0.50 p	A	A	B	B	D	D
* 0.75 p	A	A	B	B	D	D
1.0 p	A	A	B	B	D	D
1.2 p	A	A	B	B	D	D
1.5 p	A	A	B	B	D	D
1.8 p	A	A	B	B	D	D
2.2 p	A	A	B	B	D	D
2.7 p	A	A	B	B	D	D
3.3 p	A	A	B	B	D	D
3.9 p	A	A	B	B	D	D
4.7 p	A	A	B	B	D	D
5.6 p	A	A	B	B	D	D
6.8 p	A	A	B	B	D	D
8.2 p	A	A	B	B	D	D
10 p	A	A	B	B	D	D
12 p	A	A	B	B	D	D
15 p	A	A	B	B	D	D
18 p	A	A	B	B	D	D
22 p			B	B	D	D
27 p						
33 p						
39 p						
47 p						
56 p						
68 p						
82 p						
100 p						
120 p						
150 p						
180 p						
220 p						
270 p						
330 p						

Note：Thickness might be changed due to technology improvement.

Thickness Code

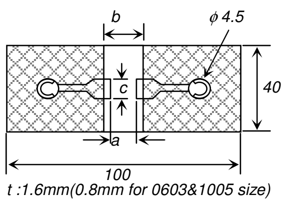
Code	Thickness (mm)
A	0.30+/-0.03
B	0.50+/-0.05
D	0.80+/-0.10

■ Taping Amount

Thickness (mm)		Amount per reel					
		180 mm (7”)		250mm (10”)		330mm (13”)	
Code	Class	Paper	Embossed	Paper	Embossed	Paper	Embossed
A	0.30 +/- 0.03	15K	X	X	X	X	X
B	0.50 +/- 0.05	10K	X	X	X	50K	X
D	0.80 +/- 0.10	4K	X	10K	X	15K	X

■ High Frequency NP0 (C0G) Specifications

	Item	Specification	Test Method
1	**Operating Temperature Range**	NP0: -55 to 125 degree C	---
2	**Rated Voltage**	16VDC, 25VDC, and 50VDC	The rated voltage is defined as the maximum voltage, which may be applied continuously to the capacitor.
3	**Appearance**	No defects or abnormalities.	Visual inspection
4	**Dimensions**	Within the specified dimension.	Using calipers
5	**Dielectric Strength (Flash)**	No defects or abnormalities.	No failure shall be observed when 250% of the rated voltage is applied between the terminations for 1 to 5 seconds. The charge and discharge current is less than 50mA.
6	**Insulation Resistance (I.R.)**	I.R.≧10GΩ	The insulation resistance shall be measured with a DC voltage not exceeding the rated voltage at 25℃ and 75%RH max, and within 1 minute of charging.
7	**Capacitance**	Within the specified tolerance	The capacitance / D.F. shall be measured at 25℃ at the frequency and voltage shown in the tables. Frequency: 1.0±0.2MHz Voltage: 1.0±0.2Vrms
8	**Quality Factor (Q)**	30pF min.: Q≧1000 30pF max.: Q≧400+20C C: Nominal Capacitance (pF)	
9	**Capacitance Temperature Characteristics**	Capacitance change within 0±30ppm/℃ under operating temperature range.	The capacitance value at 25℃ and 85℃ shall be measured and calculated from the formula given below. $T.C.=(C_{85}-C_{25})/C_{25}*\Delta T*10^{6}$(PPM/℃)
10	**Termination Strength**	No removal of the terminations or marking defect.	Apply a parallel force of 5N to a PCB mounted sample for 10±1sec. *2N for 0603 (EIA 0201).
11	**Deflection (Bending Strength)**	Appearance: No cracking or marking defects shall occur at 1mm deflection. Capacitance change: within ±2.5% or ± 0.25pF. (whichever is larger)	Solder the capacitor to the test jig (glass epoxy boards) shown in Fig.a. Using a SAC305(Sn96.5Ag3.0Cu0.5) solder. Then apply a force in the direction shown in Fig.b. The soldering shall be done with the reflow method and shall be conducted with care so that the soldering is uniform and free of defects such as heat shock.



t :1.6mm(0.8mm for 0603&1005 size)

Fig. a.

Size	a	b	C
0603	0.3	0.9	0.3
1005	0.4	1.5	0.5
1608	1.0	3.0	1.2

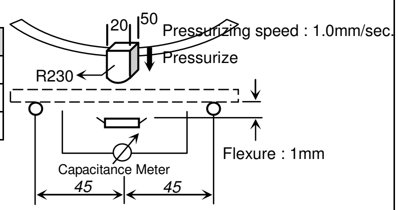


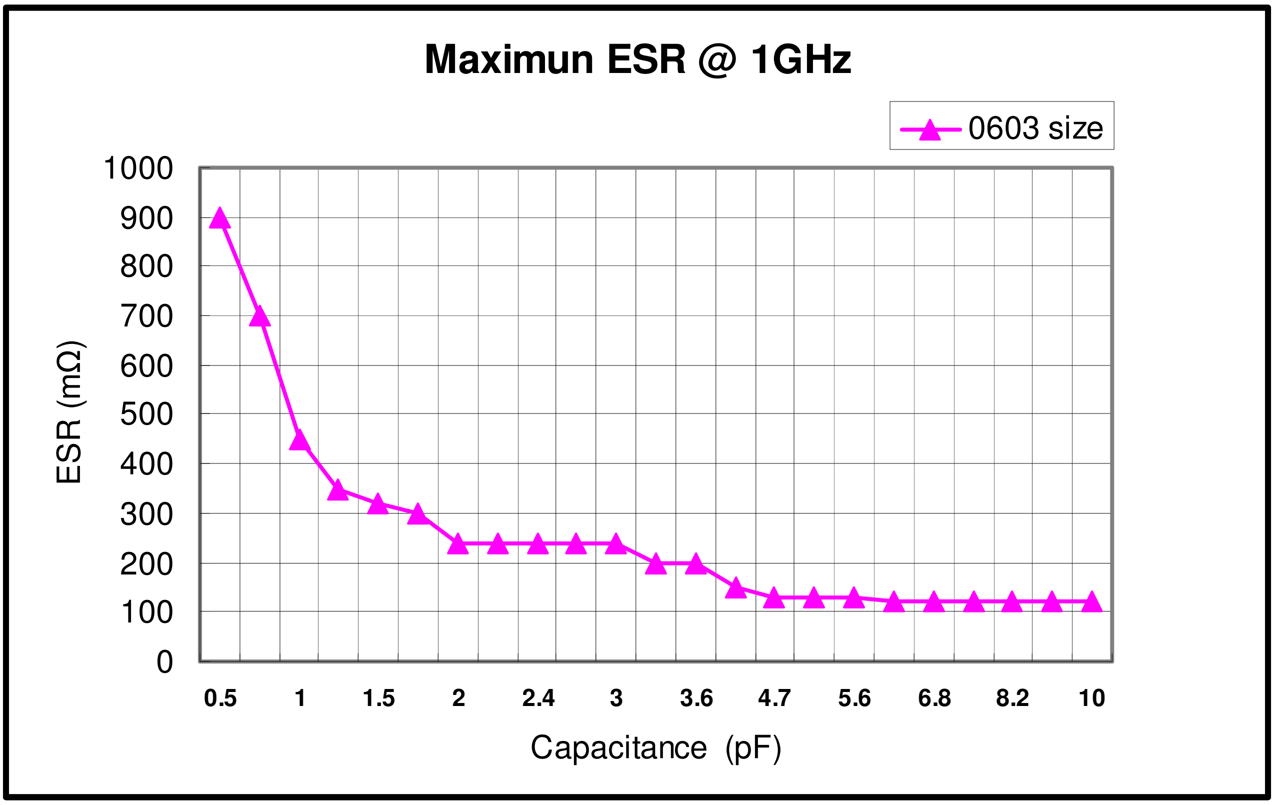
Fig. b.

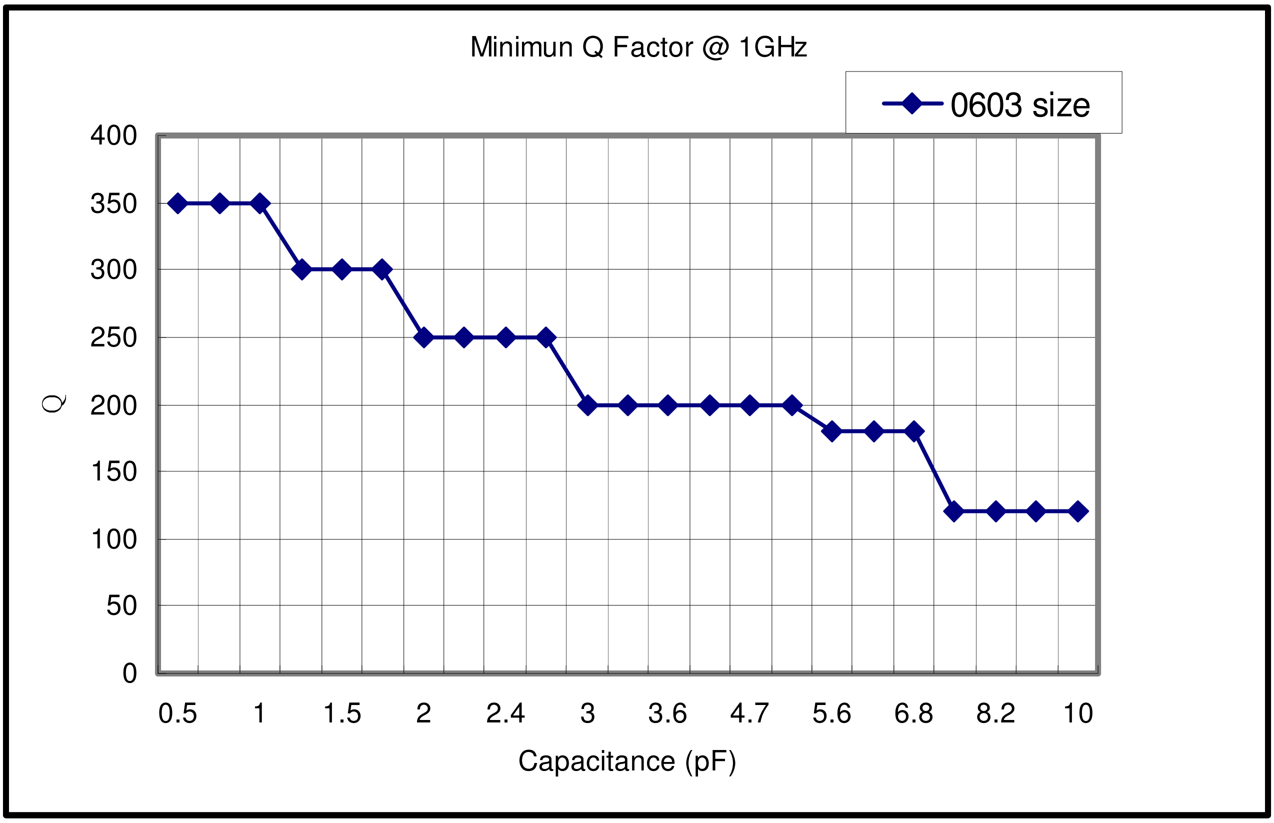
	Item		Specification	Test Method
12	**Solderability of Termination**		90% of the terminations are to be soldered evenly and continuously.	Immerse the test capacitor into a methanol solution containing rosin for 3 to 5 seconds, preheat it 150 to 180℃ for 2 to 3 minutes and immerse it into Sn-3.0Ag-0.5Cu solder of 245 ± 5 ℃ for 3±1seconds.
13	**Resistance to Soldering Heat**	**Appearance**	No marking defects	Immerse the capacitor in a SAC305(Sn96.5Ag3.0Cu0.5) solder solution at 270±5℃ for 10±1 seconds. Let sit at room temperature for 24±2 hours, then measure.
		Cap. Change	NP0 within ±2.5% or ±0.25pF (whichever is larger)	
		Q	Initial spec.	
		I.R.	Initial spec.	

Continued from previous page.

	Item		Specification	Test Method
14	Temperature cycle (Thermal shock)	Appearance	No marking defects	Solder the capacitor to supporting jig (glass epoxy board) and perform the five cycles according to the four heat treatments listed in the following table. Let sit for 24±2hrs at room temperature, then measure. Step 1: Minimum operating temperature 30±3min Step 2: Room temperature 2~3 min Step 3: Maximum operating temperature 30±3min Step 4: Room temperature 2~3min
		Cap. Change	NP0 within ±2.5% or 0.25pF (whichever is larger)	
		Q	Initial spec.	
		I.R.	Initial spec.	
15	Humidity load	Appearance	No marking defects	Apply the rated voltage at 40±2℃ and 90 to 95% humidity for 500±12 hours. Remove and let sit for 24±2 hours at room temperature, then measure. The charge / discharge current is less than 50mA.
		Cap. Change	NP0 within ±5% or ±0.5pF (whichever is larger)	
		Q	200 min.	
		I.R.	I.R.≧500MΩ	
16	High temperature load life test	Appearance	No marking defects	Apply 200% of the rated voltage for 1000±12 hours at the maximum operating temperature ± 3℃. Let sit for 24± 2 hours at room temperature, then measure. The charge/discharge current is less than 50mA.
		Cap. Change	NP0 within ±5% or ±0.5pF (whichever is larger)	
		Q	350 min.	
		I.R.	I.R.≧1GΩ	
17	RF Characteristics	Q	See **RF Characteristics of NP0 Q series P:5~7**	Measurements performed on a HP4287A with fixture 16196 and represent the typical capacitor performance.
		ESR		

■ **Typical RF Characteristics for High Frequency NP0 (C0G) 0603 (EIA 0201) at 1GHz.**

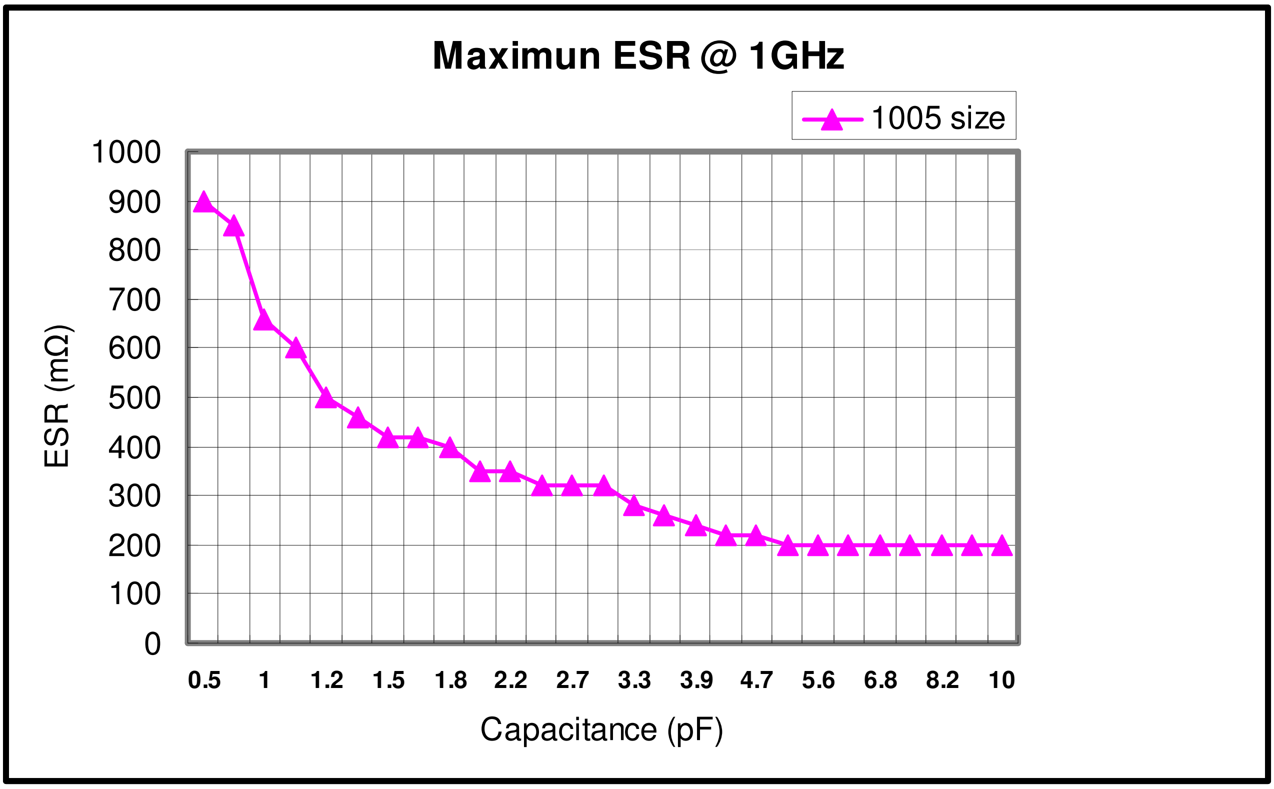


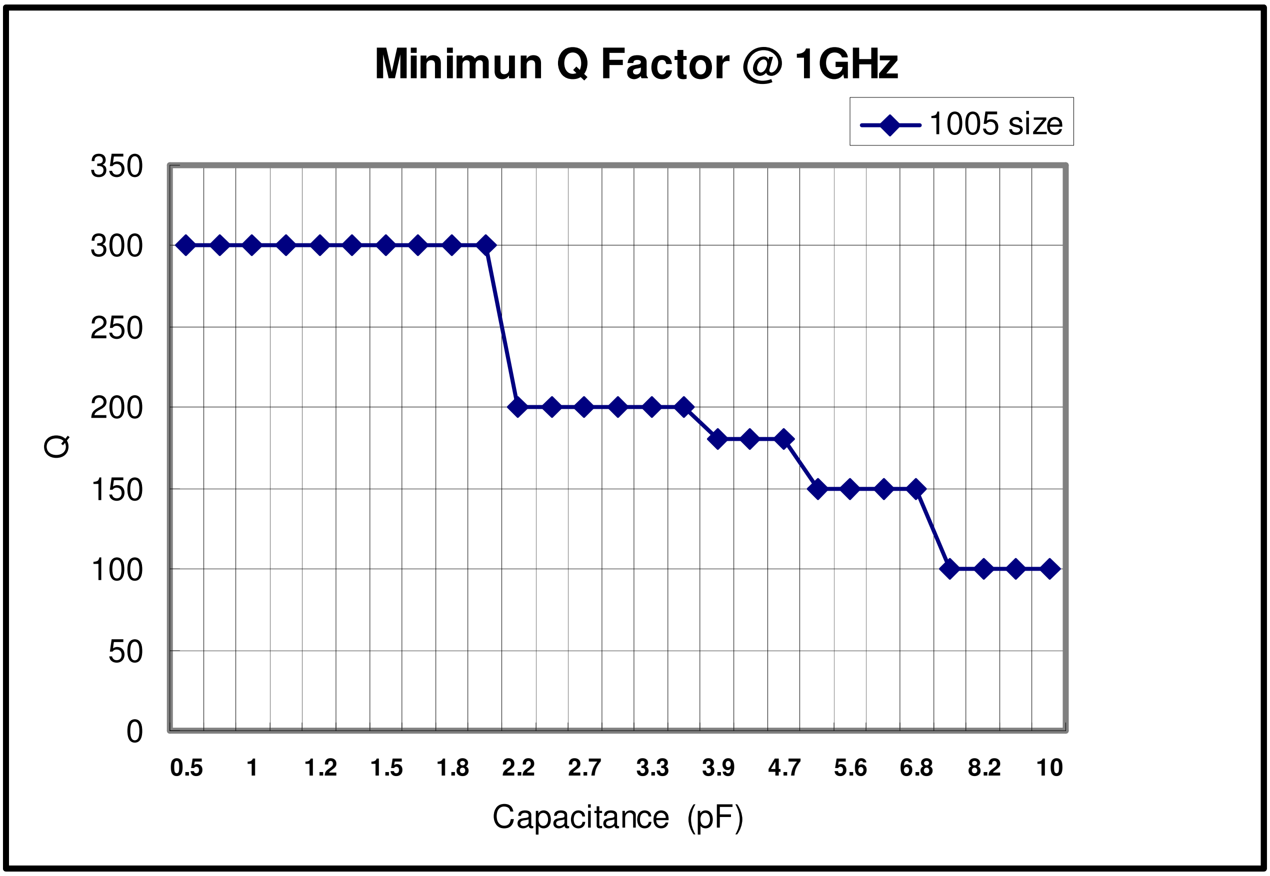


Measurements performed on a HP4287A with fixture 16196B and represent the typical capacitor performance.

S 4

■ **Typical RF Characteristics for High Frequency NP0 (C0G) 1005 (EIA 0402) at 1GHz.)**

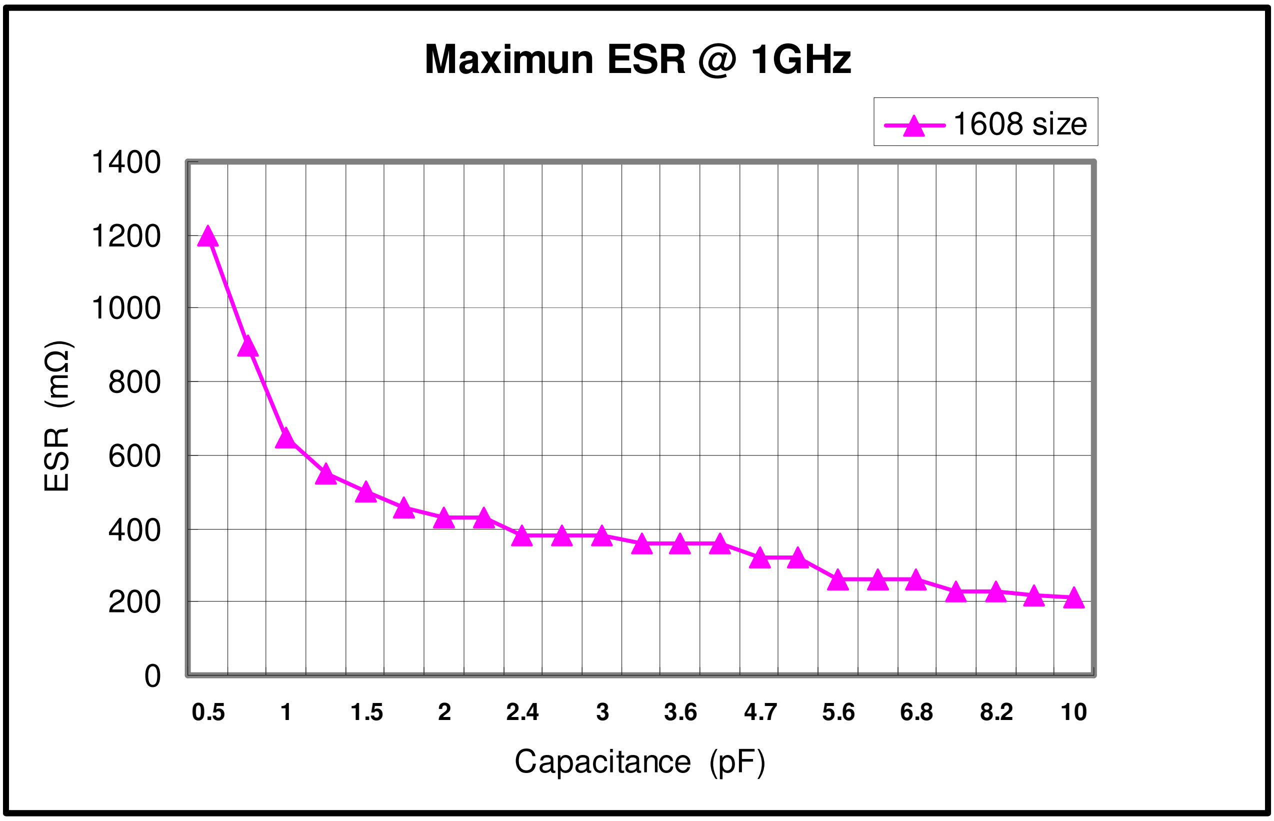


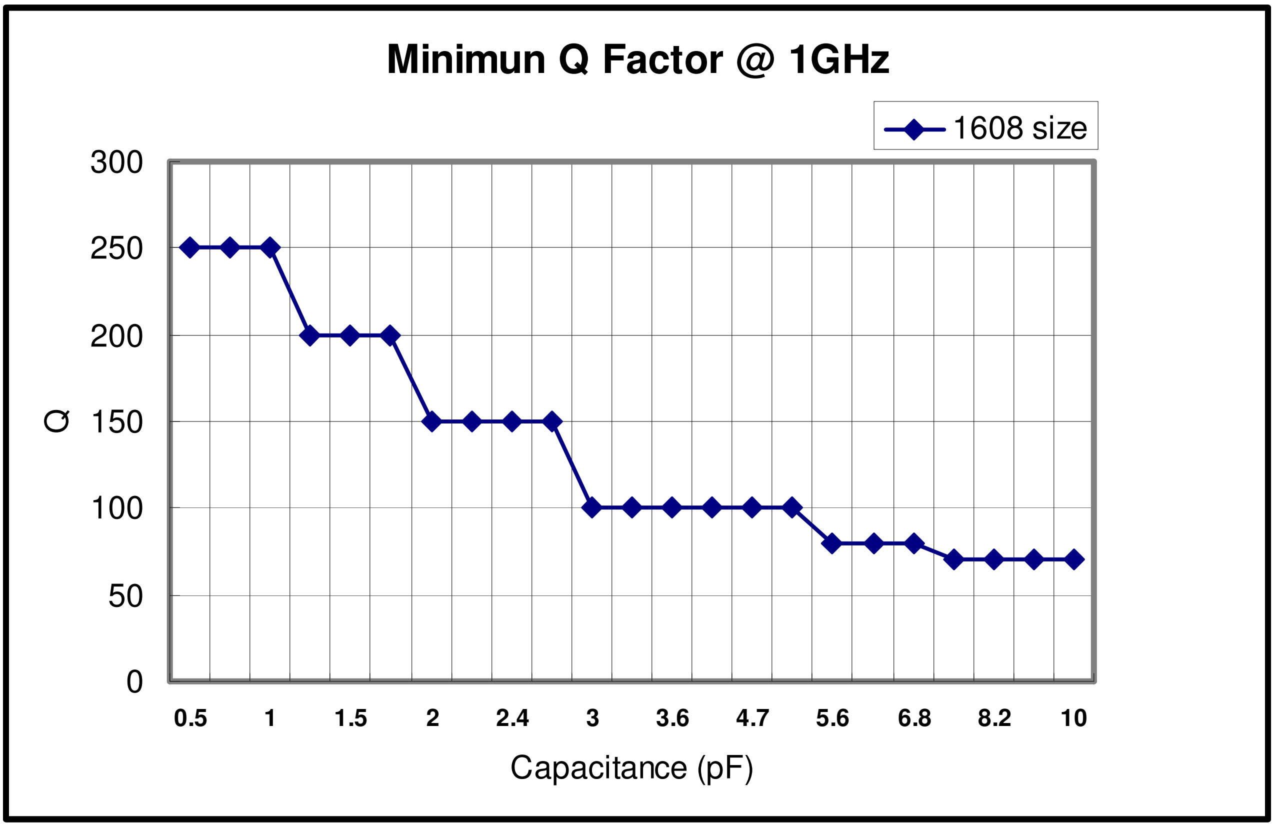


Measurements performed on a HP4287A with fixture 16196A and represent the typical capacitor performance.

S 4

■ **Typical RF Characteristics for High Frequency NP0 (C0G) 1608 (EIA 0603) at 1GHz.**



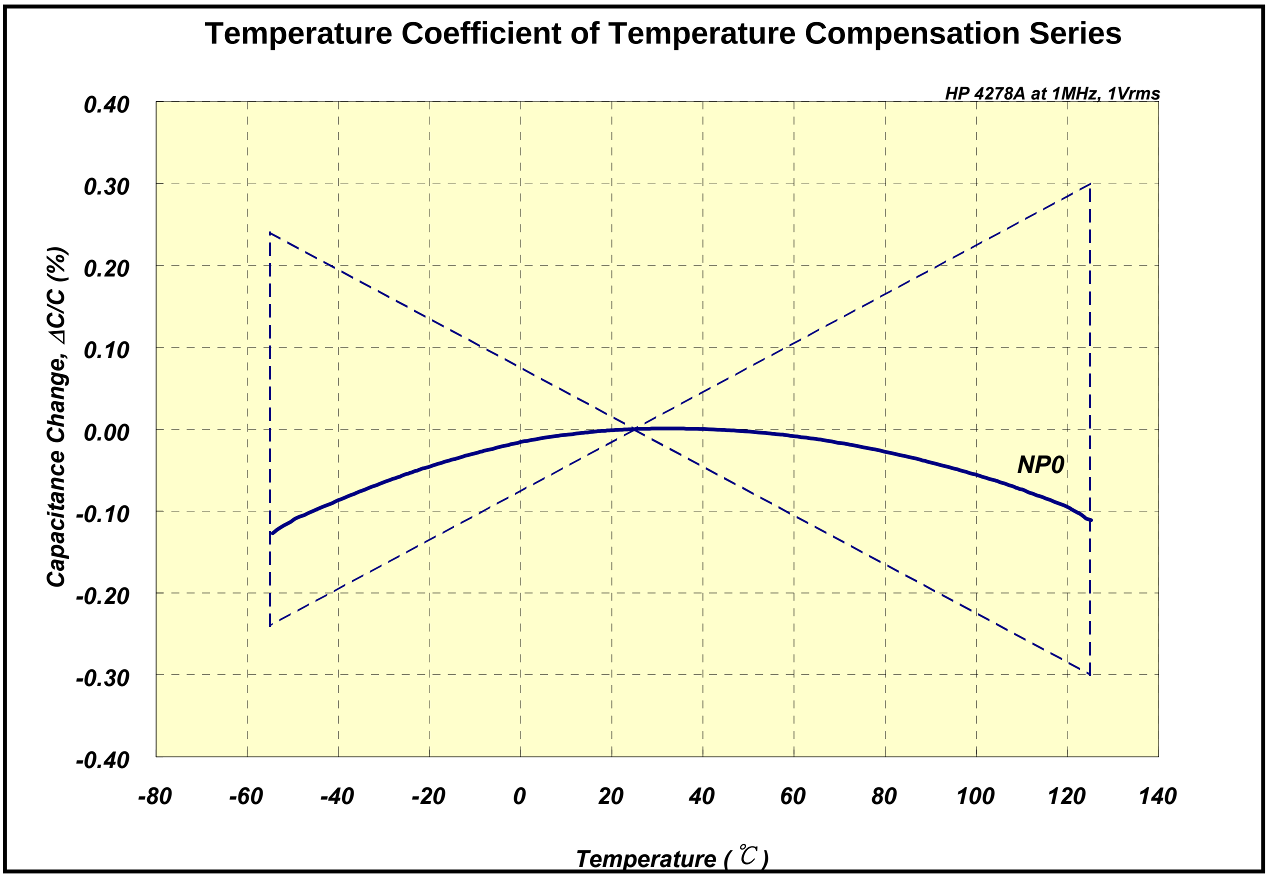


Measurements performed on a HP4287A with fixture 16196A and represent the typical capacitor performance.

Typical Characteristic Curves

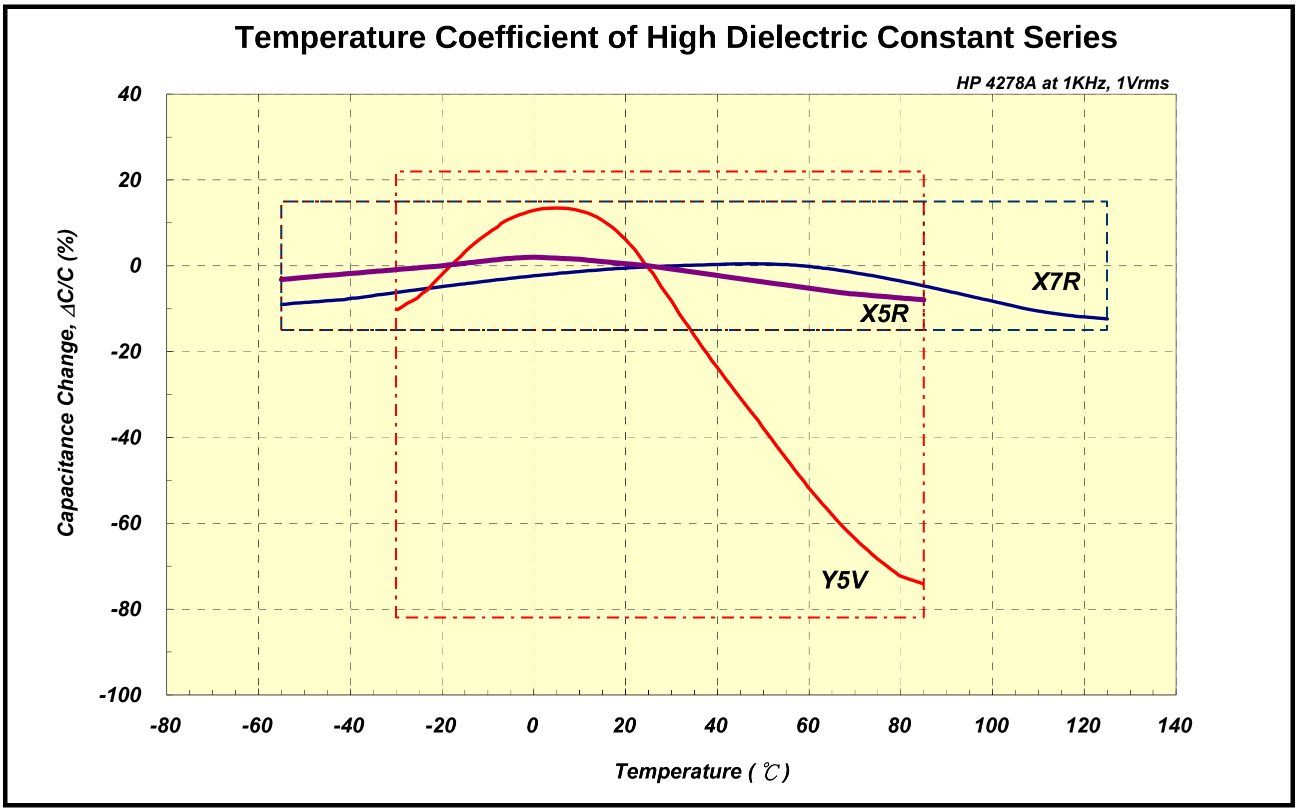
■ **Temperature Coefficient**

- **Class 1 (Temperature Compensation series)**

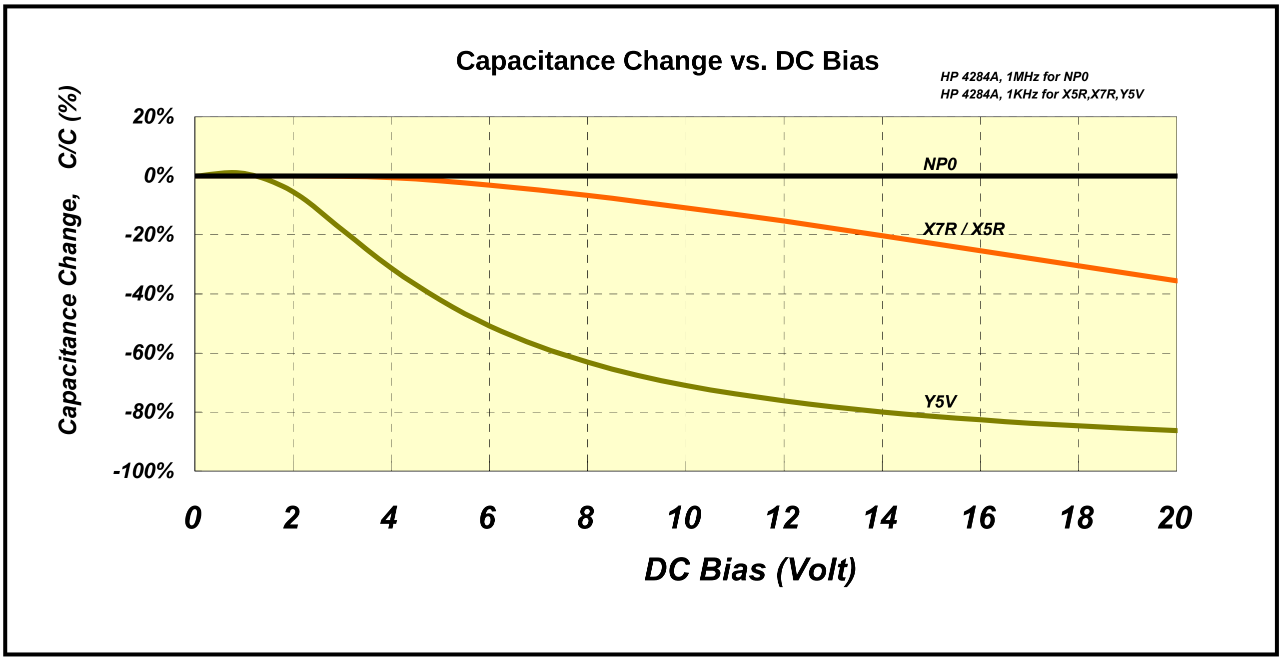


C 1

- Class 2 (High Dielectric Constant Series)

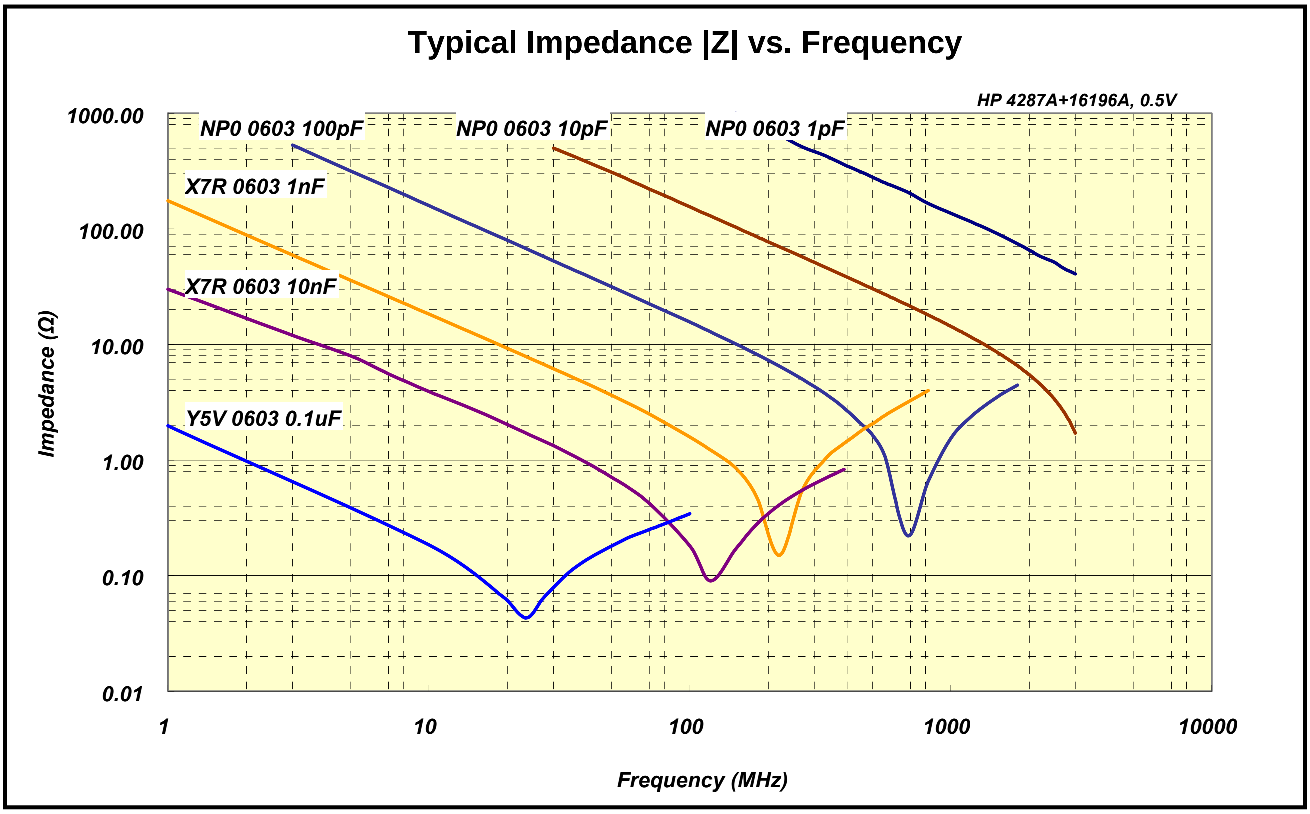


■ Capacitance Change vs. DC bias Voltage

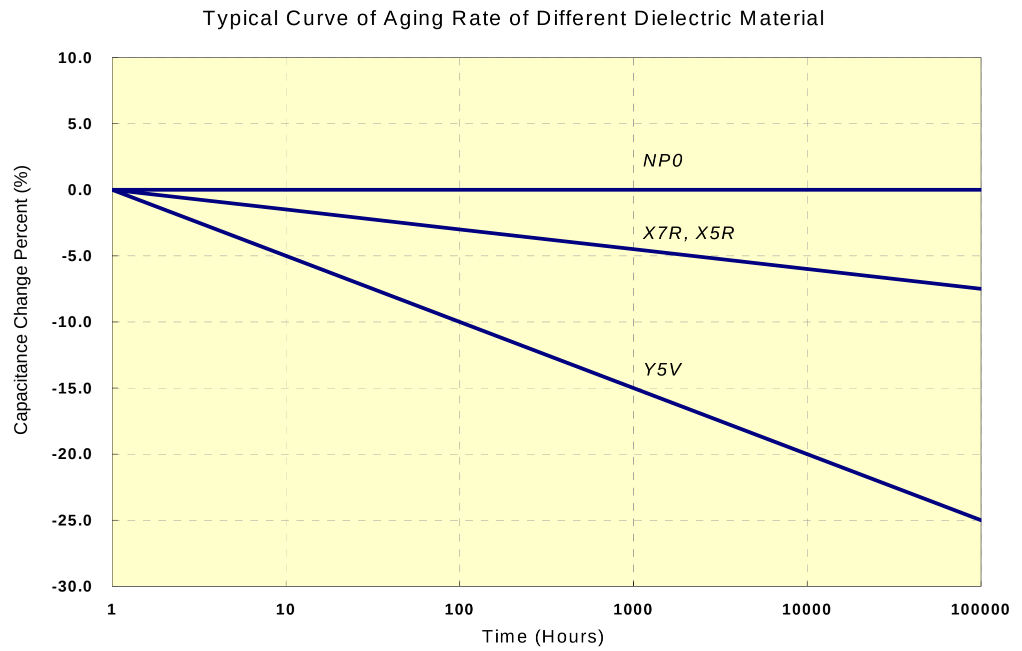


C 1

Impedance vs. Frequency



■ Aging Rate


Typical Curve of Aging Rate of Different Dielectric Material
10.0
5.0
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
Capacitance Change Percent (%)
NP0
X7R, X5R
Y5V
1
10
100
1000
10000
100000
Time (Hours)

Application Note

■ Circuit Design

1. Once application and assembly environments have been checked, the capacitor may be used in conformance with the rating and performance, which are provided in both the catalog and the specifications. Exceeding the specifications listed may result in inferior performance. It may also cause a short, open, smoking, or flaming to occur, etc.
2. Please use the capacitors in conformance with the operating temperature provided in both the catalog and the specifications. Be especially cautious not to exceed the maximum temperature. In the situation the maximum temperature set forth in both the catalog and specifications is exceeded, the capacitor's insulation resistance may deteriorate, power may suddenly surge and short-circuit may occur. The loss of capacitance will occur, and may self-heat due to equivalent series resistance when alternating electric current is passed through. As this effect becomes critical in high frequency circuits, please exercise with caution. When using the capacitor in a (self-heating) circuit, please make sure the surface of the capacitor remains under the maximum temperature for usage. Also, please make certain temperature rise remain below 20℃.
3. Please keep voltage under the rated voltage, which is applied to the capacitor. Also, please make certain the peak voltage remains below the rated voltage when AC voltage is super-imposed to the DC voltage. In the situation where AC or pulse voltage is employed, ensure average peak voltage does not exceed the rated voltage. Exceeding the rated voltage provided in both catalog and specifications may lead to defective withstanding voltage or, in worse case situations, may cause the capacitor to burn out.
4. It's is a common phenomenon of high-dielectric products to have a deteriorated amount of static electricity due to the application of DC voltage.

■ Storage

1. The chip capacitors shall be packaged in carrier tapes or bulk cases.
2. Keep storage place temperatures from +5℃ to +35℃, humidity from 45 to 70% RH.
3. The storage atmosphere must be free of gas containing sulfur and chlorine. Also, avoid exposing the product to saline moisture. If the product is exposed to such atmospheres, the terminations will oxidize and solderability will be affected.
4. The solderability is assured for 12 months from our final inspection date if the above storage condition is followed.

Handling

Chip capacitors should be handled with care to avoid contamination or damage. The use of vacuum pick-up or plastic tweezers is recommended for manual placement. Tape and reeled packages are suitable for automatic pick and placement machine.

Flux

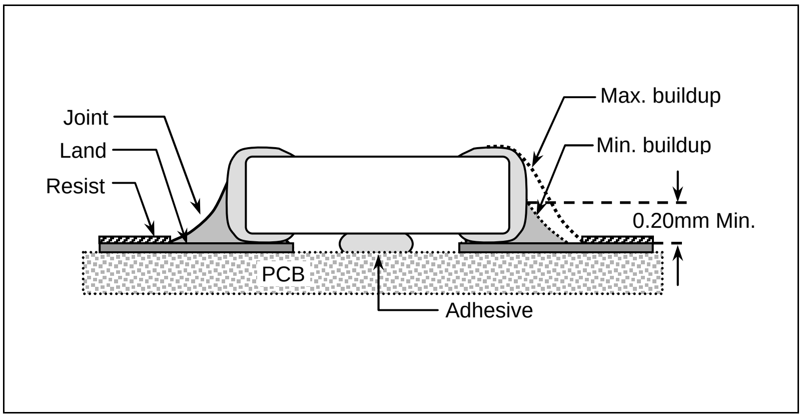
1. An excessive amount of flux or too rapid temperature rise can causes solvent burst, solder can generate a large quantity of gas. The gas can spreads small solder particles to cause solder balling effect or bridging problem.
2. Flux containing too high of a percentage of halide may cause corrosion of termination unless sufficient cleaning is applied.
3. Use rosin-type flux. Highly acidic flux (halide content less than 0.2wt%) is not recommended.
4. The water soluble flux causes deteriorated insulation resistance between outer terminations unless sufficiently cleaned.

Component Spacing

For wave soldering components, the spacing must be sufficient far apart to prevent bridging or shadowing. This is not so important for reflow process but sufficient space for rework should be considered. The suggested spacing for reflow soldering and wave soldering is 0.5mm and 1.0mm, respectively.

Solder Fillet

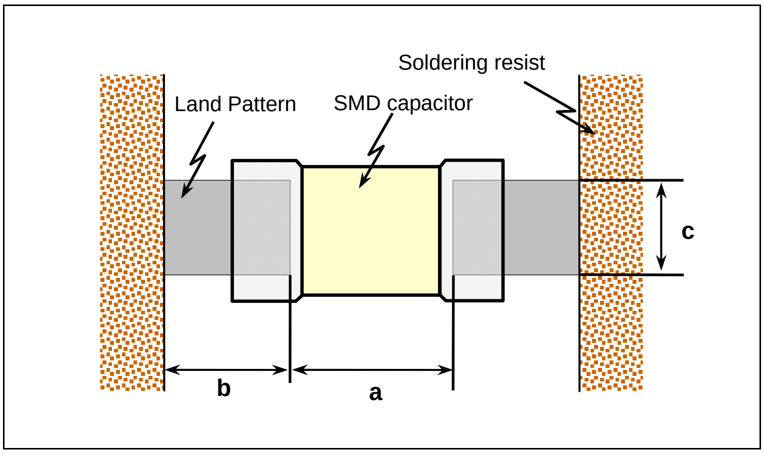
Too much solder amount may increase solder stress and cause crack risk. Insufficient solder amount may reduce adhesive strength and cause parts falling off PCB. When soldering, confirm that the solder is placed over 0.2mm of the surface of the terminations.



Recommended Land Pattern Dimensions

When mounting the capacitor to substrate, it's important to consider carefully that the amount of solder (size of fillet) used has a direct effect upon the capacitor once it's mounted.

1. The greater the amount of solder, the greater the stress to the elements. As this may cause the substrate to break or crack.
2. In the situation where two or more devices are mounted onto a common land separate the device into exclusive pads by using soldering resist.
3. Land width equal to or less than component. It is permissible to reduce land width to 80% of component width.



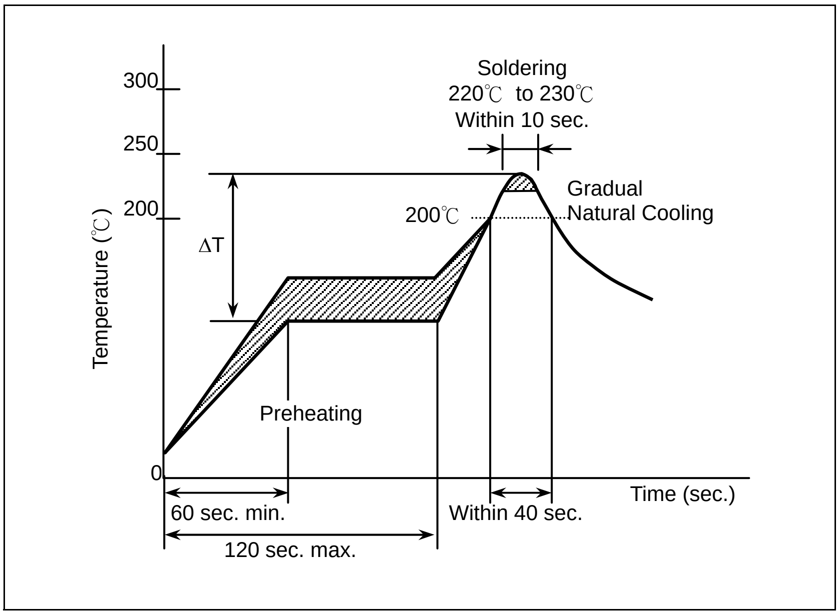
Size mm (EIA)	L x W (mm)	a (mm)	b (mm)	c (mm)
0603 (0201)	0.6*0.3	0.15 to 0.35	0.2 to 0.3	0.25 to 0.3
1005 (0402)	1.0*0.5	0.3 to 0.5	0.35 to 0.45	0.4 to 0.5
1608 (0603)	1.6*0.8	0.7 to 1.0	0.6 to 0.8	0.7 to 0.8
2012 (0805)	2.0*1.25	1.0 to 1.3	0.7 to 0.9	1.0 to 1.2
3216 (1206)	3.2*1.6	2.1 to 2.5	1.0 to 1.2	1.3 to 1.6
3225 (1210)	3.2*2.5	2.1 to 2.5	1.0 to 1.2	2.0 to 2.5
4520 (1808)	4.5*2.0	3.2 to 3.8	1.2 to 1.4	1.7 to 2.0
4532 (1812)	4.5*3.2	3.2 to 3.8	1.2 to 1.4	2.7 to 3.2

■ Resin Mold

If a large amount of resin is used for molding the chip, cracks may occur due to contraction stress during curing. To avoid such cracks, use a low shrinkage resin. The insulation resistance of the chip will degrade due to moisture absorption. Use a low moisture absorption resin. Check carefully that the resin does not generate a decomposition gas or reaction gas during the curing process or during normal storage. Such gases may crack the chip capacitor or damage the device itself.

■ Soldering Profile for SMT Process with SnPb Solder Paste

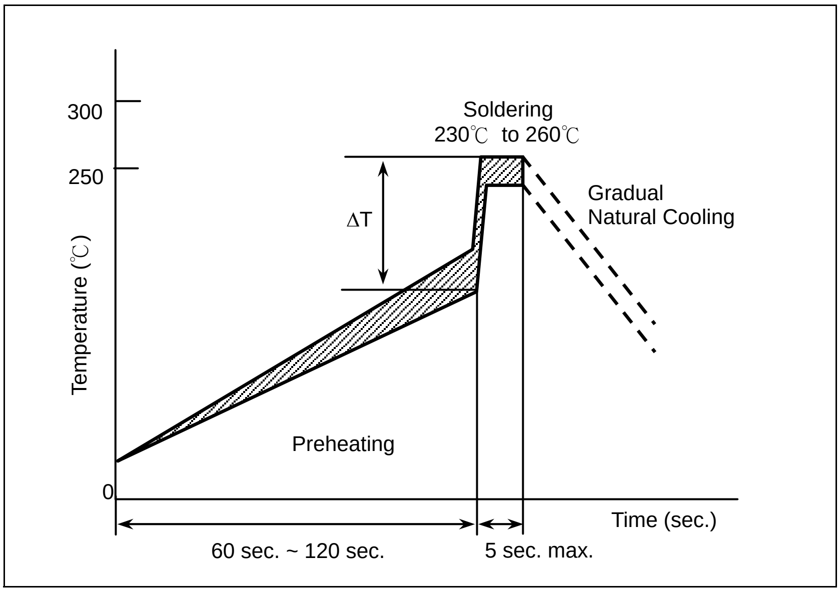
● Reflow Soldering



The difference between solder and chip surface should be controlled as following table. The rate of preheat should not exceed 4℃/sec and a target of 2℃/sec is preferred.

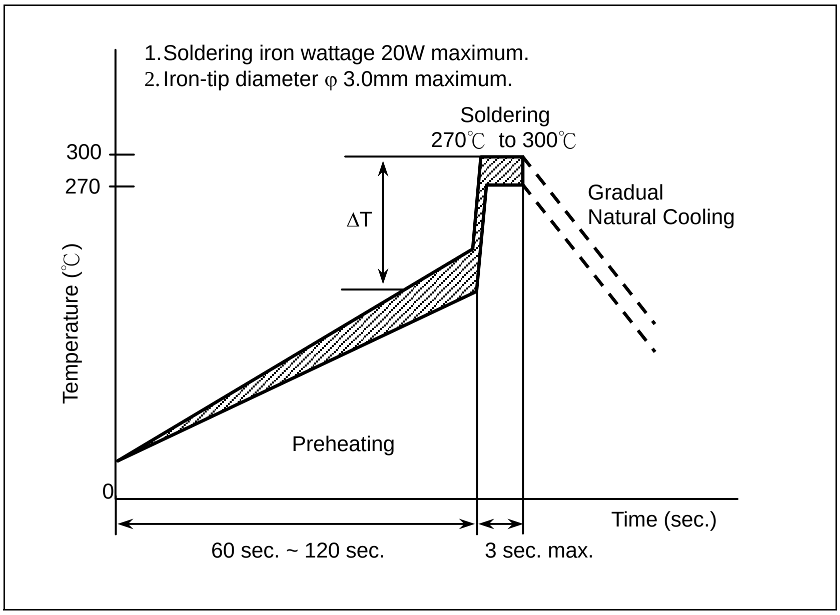
Chip Size	3216 and smaller	3225 and above
Preheating	ΔT≤150℃	ΔT≤130℃

- **Wave Soldering**



Chip Size	3216 and smaller	3225 and above
Preheating	ΔT≤150℃	-

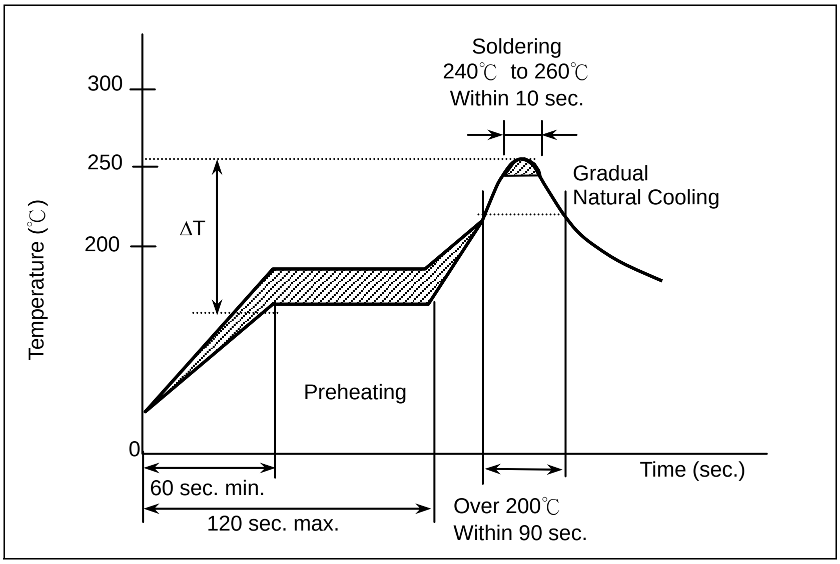
- **Soldering Iron**



Chip Size	3216 and smaller	3225 and above
Preheating	ΔT≤190℃	ΔT≤130℃

■ Soldering

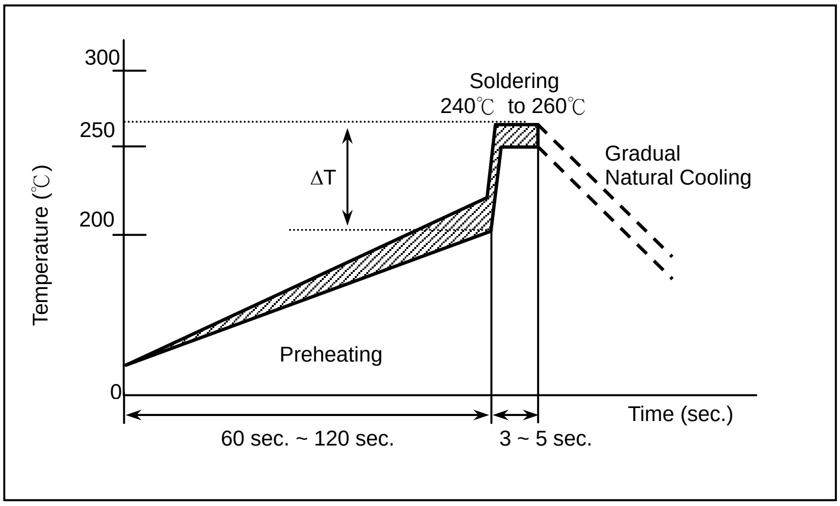
- **Reflow Soldering for Lead free Termination**



The difference between solder and chip surface should be controlled as following table. The rate of preheat should not exceed 4℃/sec and a target of 2℃/sec is preferred.

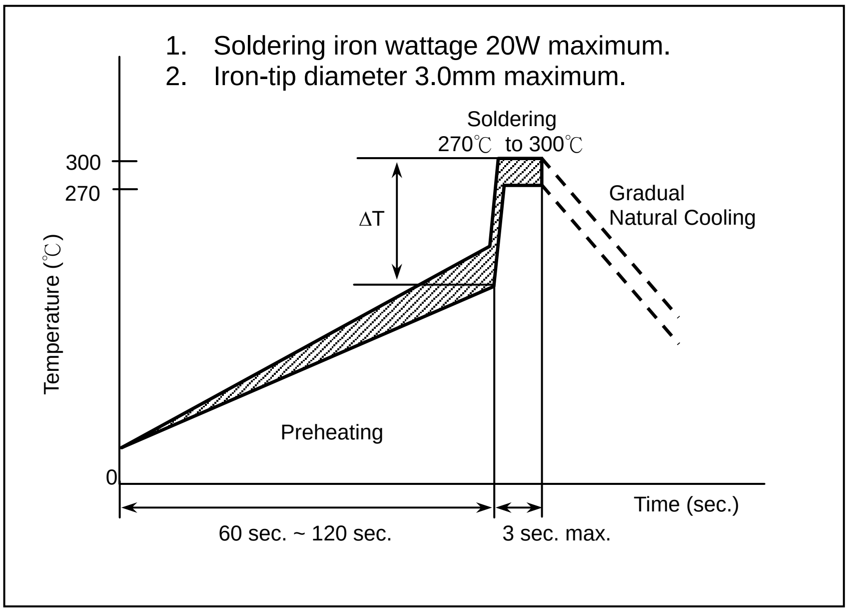
Chip Size	3216 and smaller	3225 and above
Preheating	ΔT≤150℃	ΔT≤130℃

- **Flow Soldering for Lead free Termination**



Chip Size	3216 and smaller	3225 and above
Preheating	ΔT≤150℃	-

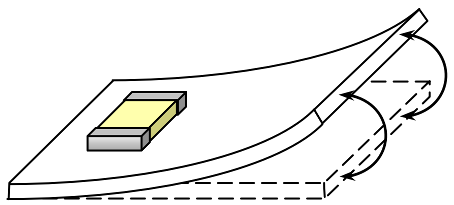
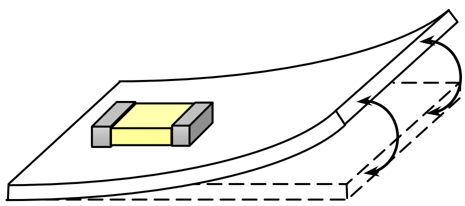
- **Soldering Iron**



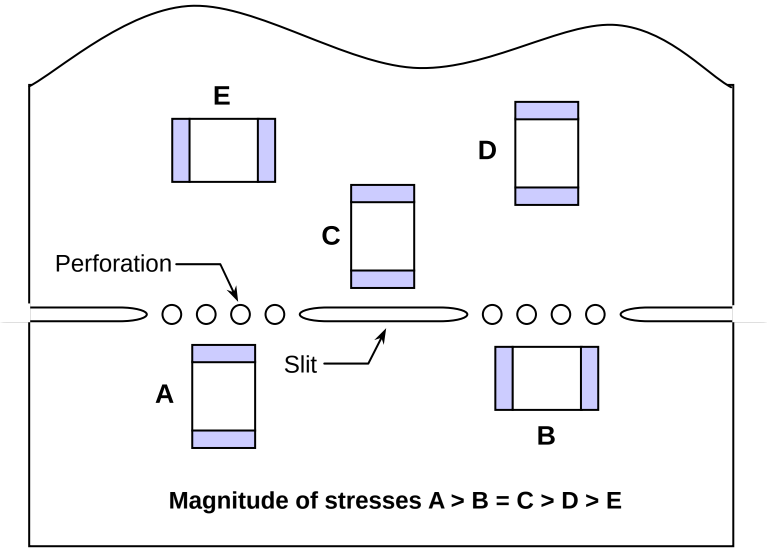
Chip Size	3216 and smaller	3225 and above
Preheating	ΔT≤190℃	ΔT≤130℃

Chip Layout and Breaking PCB

1. To layout the SMD capacitors for reducing bend stress from board deflection of PCB. The following are examples of good and bad layout.

Recommended	Not Recommended
	

2. When breaking PCB, the layout should be noted that the mechanical stresses are depending on the position of capacitors. The following example shows recommendation for better design.



■ Aging

The capacitance and dissipation factor of class 2 capacitors decreases with time. It is known as 'aging' that follows a logarithmic low and expressed in terms of an aging constant. Aging is caused by a gradual re-alignment of the crystalline structure of the ceramic. The aging constant is defined as the percentage loss of capacitance at a 'time decade'. The law of capacitance aging is expressed as following equation:

$C_{t2} = C_{t1} \times (1 - k \times \log_{10}(t_2/t_1))$

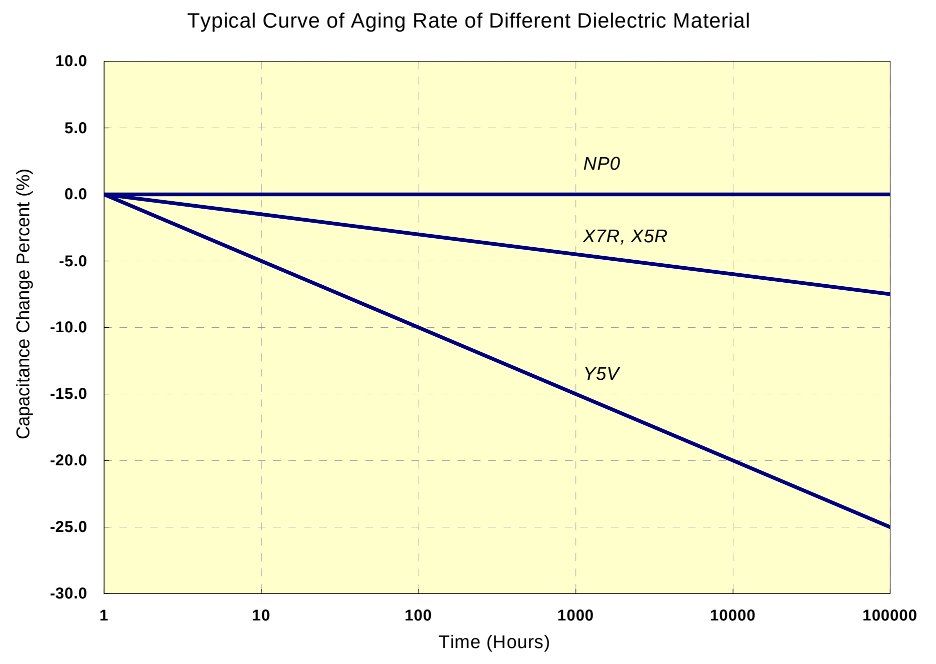
C_{t1}: *Capacitance after t1 hours of start aging.*

C_{t2}: *Capacitance after t2 hours of start aging.*

k: aging constant (capacitance decrease per decade)

t1, t2: time in hours from start of aging.

A typical curve of aging rate is shown in following figure.



When heating the capacitors above Curie temperature (130℃~150℃) the capacitance can be re-new. So capacitance of class 2 capacitors will be complete de-aged by soldering process; subsequently a new aging process begins.

Because of aging, it is specified an age for measurement to meet the prescribed tolerance for class 2 capacitors. Normally, 1000 hours (t_2=1000 hrs) is defined.